IN THE CLAIMS

Please amend the claims as follows:

Claims 1-8 (Cancelled)

9. (New) Device for synchronizing a sampling clock in the case of sampling digital signals comprising:

a phase lock loop (PLL) which multiplies a signal at a given frequency by an integer number, said PLL receiving a reference signal at an input thereof and outputting a clock signal,

means for formulating n analysis zones, said formulating means receiving the clock signal at an input and outputting signals determining the n analysis zones,

an analysis circuit for comparing, during a specified time, digital signals to signals determining the n analysis zones, counting by zone the results of the comparisons then testing the results of the comparisons in order to send either a phase correction signal to an input of a comparator, the other input receiving the reference signal and the output being connected to the PLL input or a frequency correction circuit sent to the input of the PLL to modify the integer number.

10. (New) Device according to claim 9, wherein the formulating means comprises a circuit in combinatorial logic treating the clock signal from the PLL to generate windows in combinatorial logic to produce the n analysis zones.

11. (New) Device according to claim 10, wherein the windows respectively correspond to the rising and falling transitions of the sampling clock.

12. (New) Device according to claim 9, wherein the formulating means formulates four zones wherein a first zone corresponds to a rising transition, a second zone

corresponds to a falling transition, a third zone corresponds to a top porch and a fourth zone corresponds to a bottom porch.

13. (New) Device according to claim 9, wherein the analysis circuit is constituted by an erasable programmable electronic circuit.

14. (New) Device according to claim 9, wherein the analysis circuit comprises

a plurality of counters, each counter being associated with a respective zone, each counter counting the number of transitions by zone, being reset at the beginning of each analysis time and being able to count up to a maximal cumulative value;

a plurality of decoding circuits, each decoding circuit connected to an output of a respective counter; and

a testing circuit connected to an output of each of the plurality of decoding circuits, said testing circuit sending signals to a first counter, the output of said first counter being sent to a circuit giving the value of the frequency correction signal and to a pulse modulation circuit giving the value of the phase correction signal.

15. (New) Device according to claim 14, wherein the pulse modulation circuit comprises a first up/down counter and a second counter counting up to a given maximum value.

16. (New) Device according to claim 14, wherein the testing circuit compares the output value of each decoding circuit and determines in relation with the relative output values of two different decoding circuits or with the output value of an decoding circuit different from the specific analysis circuit corresponding to a specific transition in the clock signal, the direction and the magnitude of the phase correction signal or of the frequency correction signal to apply on the clock signal.